1. (Twice amended) A method of forming a microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of:

(a) forming a first polymeric material on a surface of a semiconductor wafer having interconnect pads disposed thereon;

(b) patterning said first polymeric material to provide openings that expose said interconnect pads;

(c) forming conductive bump material in said openings;

(d) forming a second polymeric material that is partially cured to a B-stage state over said first polymeric material and said conductive bump material;

(e) dicing said semiconductor wafer into individual chips; and

(f) bonding at least one of said individual chips to an external substrate, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate.

REMARK

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested.

Applicants acknowledge, with thanks, the Examiner's indication in the Final Rejection dated December 4, 2002 that Claims 21-22 are allowable over the art of record. Although allowance of Claims 21-22 is indicated, applicants, at the present time, would like to obtain a patent including all the claims pending in the present application.

Before addressing the specific rejection raised in the Final Rejection dated December 4, 2002, applicants have amended Claim 1. Claim 1 has been amended to clearly and positively